

# Am73/8303 • Am73/8304B

Octal Three-State Bidirectional Bus Transceivers

## DISTINCTIVE CHARACTERISTICS

- 8-bit bidirectional data flow reduces system package count
- 3-state inputs/outputs for interfacing with bus-oriented systems
- PNP inputs reduce input loading
- $V_{CC} - 1.15V$   $V_{OH}$  interfaces with TTL, MOS and CMOS
- 48mA, 300pF bus drive capability
- Am73/8303 inverting transceivers
- Am73/8304B noninverting transceivers
- Transmit/Receive and Chip Disable simplify control logic
- 20-pin ceramic and molded DIP package
- Low power – 8mA per bidirectional bit
- Advanced Schottky processing
- Bus port stays in hi-impedance state during power up/down
- 100% product assurance screening to MIL-STD-883 requirements

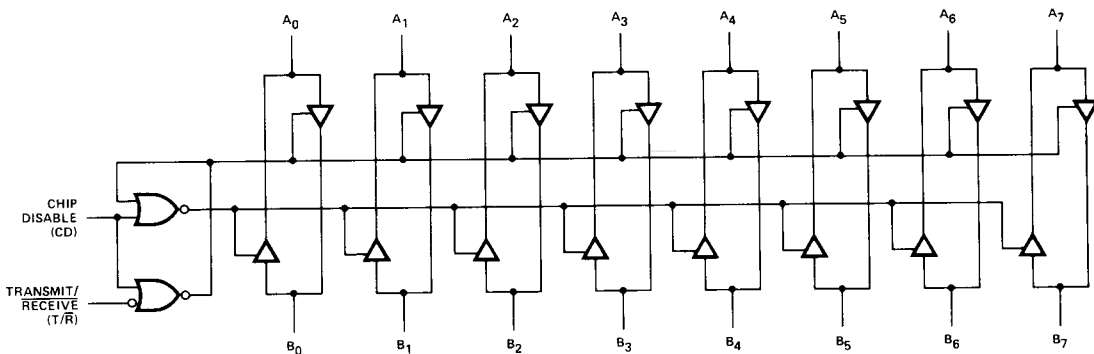
## FUNCTIONAL DESCRIPTION

The Am73/8303 and Am73/8304B are 8-bit 3-State Schottky transceivers. They provide bidirectional drive for bus-oriented microprocessor and digital communications systems. Straight through bidirectional transceivers are featured, with 16mA drive capability on the A ports and 48mA bus drive capability on the B ports. PNP inputs are incorporated to reduce input loading.

One input, Transmit/Receive determines the direction of logic signals through the bidirectional transceiver. The Chip Disable input disables both A and B ports by placing them in a 3-state condition. Chip Disable is functionally the same as an active LOW chip select.

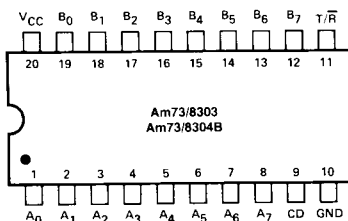
The output high voltage ( $V_{OH}$ ) is specified at  $V_{CC} - 1.15V$  minimum to allow interfacing with MOS, CMOS, TTL, ROM, RAM, or microprocessors.

Am73/8304B  
LOGIC DIAGRAM



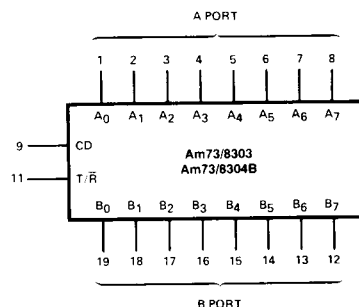
Am73/8303 has inverting transceivers

CONNECTION DIAGRAM  
Top View



Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



$V_{CC}$  = Pin 20  
GND = Pin 10

12

**ABSOLUTE MAXIMUM RATINGS** (Above which the useful life may be impaired)

Storage Temperature	-65 to +150°C
Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Lead Temperature (Soldering, 10 seconds)	300°C

**ELECTRICAL CHARACTERISTICS**

The Following Conditions Apply Unless Otherwise Noted:

MIL	$T_A = -55$ to $+125^\circ\text{C}$	$V_{CC}$ MIN = 4.5V	$V_{CC}$ MAX = 5.5V
COM'L	$T_A = 0$ to $+70^\circ\text{C}$	$V_{CC}$ MIN = 4.75V	$V_{CC}$ MAX = 5.25V

**DC ELECTRICAL CHARACTERISTICS** over operating temperature range

Parameters	Description	Test Conditions	Min	Typ (Note 1)	Max	Units
<b>A PORT (A<sub>0</sub>-A<sub>7</sub>)</b>						
$V_{IH}$	Logical "1" Input Voltage	$CD = V_{IL}$ MAX, $T/\bar{R} = 2.0V$	2.0			Volts
$V_{IL}$	Logical "0" Input Voltage	$CD = V_{IL}$ MAX, $T/\bar{R} = 2.0V$			0.8 0.7	Volts
$V_{OH}$	Logical "1" Output Voltage	$CD = V_{IL}$ MAX, $T/\bar{R} = 0.8V$	$I_{OH} = -0.4mA$	$V_{CC} - 1.15$	$V_{CC} - 0.7$	Volts
			$I_{OH} = -3.0mA$	2.7	3.95	
$V_{OL}$	Logical "0" Output Voltage	$CD = V_{IL}$ MAX, $T/\bar{R} = 0.8V$	$I_{OL} = 8mA$		0.3 0.4	Volts
			COM'L $I_{OL} = 16mA$		0.35 0.50	
$I_{OS}$	Output Short Circuit Current	$CD = V_{IL}$ MAX, $T/\bar{R} = 0.8V$ , $V_O = 0V$ , $V_{CC} =$ MAX, Note 2	-10	-38	-75	mA
$I_{IH}$	Logical "1" Input Current	$CD = V_{IL}$ MAX, $T/\bar{R} = 2.0V$ , $V_I = 2.7V$		0.1	80	$\mu A$
$I_I$	Input Current at Maximum Input Voltage	$CD = 2.0V$ , $V_{CC}$ MAX, $V_I = V_{CC}$ MAX			1	mA
$I_{IL}$	Logical "0" Input Current	$CD = V_{IL}$ MAX, $T/\bar{R} = 2.0V$ , $V_I = 0.4V$		-70	-200	$\mu A$
$V_C$	Input Clamp Voltage	$CD = 2.0V$ , $I_{IN} = -12mA$		-0.7	-1.5	Volts
$I_{OD}$	Output/Input 3-State Current	$CD = 2.0V$	$V_O = 0.4V$		-200	$\mu A$
			$V_O = 4.0V$		80	
<b>B PORT (B<sub>0</sub>-B<sub>7</sub>)</b>						
$V_{IH}$	Logical "1" Input Voltage	$CD = V_{IL}$ MAX, $T/\bar{R} = V_{IL}$ MAX	2.0			Volts
$V_{IL}$	Logical "0" Input Voltage	$CD = V_{IL}$ MAX, $T/\bar{R} = V_{IL}$ MAX			0.8 0.7	Volts
$V_{OH}$	Logical "1" Output Voltage	$CD = V_{IL}$ MAX, $T/\bar{R} = 2.0V$	$I_{OH} = -0.4mA$	$V_{CC} - 1.15$	$V_{CC} - 0.8$	Volts
			$I_{OH} = -5.0mA$	2.7	3.9	
			$I_{OH} = -10mA$	2.4	3.6	
$V_{OL}$	Logical "0" Output Voltage	$CD = V_{IL}$ MAX, $T/\bar{R} = 2.0V$	$I_{OL} = 20mA$		0.3 0.4	Volts
			$I_{OL} = 48mA$		0.4 0.5	
$I_{OS}$	Output Short Circuit Current	$CD = V_{IL}$ MAX, $T/\bar{R} = 2.0V$ , $V_O = 0V$ , $V_{CC} =$ MAX, Note 2	-25	-50	-150	mA
$I_{IH}$	Logical "1" Input Current	$CD = V_{IL}$ MAX, $T/\bar{R} = V_{IL}$ MAX, $V_I = 2.7V$		0.1	80	$\mu A$
$I_I$	Input Current at Maximum Input Voltage	$CD = 2.0V$ , $V_{CC} =$ MAX, $V_I = V_{CC}$ MAX			1	mA
$I_{IL}$	Logical "0" Input Current	$CD = V_{IL}$ MAX, $T/\bar{R} = V_{IL}$ MAX, $V_I = 0.4V$		-70	-200	$\mu A$
$V_C$	Input Clamp Voltage	$CD = 2.0V$ , $I_{IN} = -12mA$		-0.7	-1.5	Volts
$I_{OD}$	Output/Input 3-State Current	$CD = 2.0V$	$V_O = 0.4V$		-200	$\mu A$
			$V_O = 4.0V$		200	
<b>CONTROL INPUTS <math>CD</math>, <math>T/\bar{R}</math></b>						
$V_{IH}$	Logical "1" Input Voltage		2.0			Volts
$V_{IL}$	Logical "0" Input Voltage				0.8	Volts
		COM'L MIL			0.7	
$I_{IH}$	Logical "1" Input Current	$V_I = 2.7V$		0.5	20	$\mu A$
$I_I$	Input Current at Maximum Input Voltage	$V_{CC} =$ MAX, $V_I = V_{CC}$ MAX			1.0	mA
$I_{IL}$	Logical "0" Input Current	$V_I = 0.4V$	$T/\bar{R}$		-0.1 -0.25	mA
			CD		-0.1 -0.25	
$V_C$	Input Clamp Voltage	$I_{IN} = -12mA$		-0.8	-1.5	Volts
<b>POWER SUPPLY CURRENT</b>						
$I_{CC}$	Power Supply Current	Am73/8303	$CD = V_I = 2.0V$ , $V_{CC} =$ MAX	70	100	mA
			$CD = 0.4V$ , $V_{INA} = T/\bar{R} = 2.0V$ , $V_{CC} =$ MAX	100	150	
		Am73/8304B	$CD = 2.0V$ , $V_I = 0.4V$ , $V_{CC} =$ MAX	70	100	mA
			$CD = V_{INA} = 0.4V$ , $T/\bar{R} = 2.0V$ , $V_{CC} =$ MAX	90	140	

AC ELECTRICAL CHARACTERISTICS ( $V_{CC} = 5.0V$ ,  $T_A = 25^\circ C$ )

Parameters	Description	Test Conditions	Typ (Note 1)	Max	Units
<b>A PORT DATA/MODE SPECIFICATIONS</b>					
$t_{PDHLA}$	Propagation Delay to a Logical "0" from B Port to A Port	$CD = 0.4V$ , $T/\bar{R} = 0.4V$ (Figure 1) $R_1 = 1k$ , $R_2 = 5k$ , $C_1 = 30pF$	8	12	ns
$t_{PDLHA}$	Propagation Delay to a Logical "1" from B Port to A Port	$CD = 0.4V$ , $T/\bar{R} = 0.4V$ (Figure 1) $R_1 = 1k$ , $R_2 = 5k$ , $C_1 = 30pF$	11	16	ns
$t_{PLZA}$	Propagation Delay from a Logical "0" to 3-State from CD to A Port	$B_0$ to $B_7 = 2.4V$ , $T/\bar{R} = 0.4V$ (Figure 3) $S_3 = 1$ , $R_5 = 1k$ , $C_4 = 15pF$	10	15	ns
$t_{PHZA}$	Propagation Delay from a Logical "1" to 3-State from CD to A Port	$B_0$ to $B_7 = 0.4V$ , $T/\bar{R} = 0.4V$ (Figure 3) $S_3 = 0$ , $R_5 = 1k$ , $C_4 = 15pF$	8	15	ns
$t_{PZLA}$	Propagation Delay from 3-State to a Logical "0" from CD to A Port	$B_0$ to $B_7 = 2.4V$ , $T/\bar{R} = 0.4V$ (Figure 3) $S_3 = 1$ , $R_5 = 1k$ , $C_4 = 30pF$	20	30	ns
$t_{PZHA}$	Propagation Delay from 3-State to a Logical "1" from CD to A Port	$B_0$ to $B_7 = 0.4V$ , $T/\bar{R} = 0.4V$ (Figure 3) $S_3 = 0$ , $R_5 = 5k$ , $C_4 = 30pF$	19	30	ns
<b>B PORT DATA/MODE SPECIFICATIONS</b>					
$t_{PDHLB}$	Propagation Delay to a Logical "0" from A Port to B Port	$CD = 0.4V$ , $T/\bar{R} = 2.4V$ (Figure 1) $R_1 = 100\Omega$ , $R_2 = 1k$ , $C_1 = 300pF$	12	18	ns
		$R_1 = 667\Omega$ , $R_2 = 5k$ , $C_1 = 45pF$	7	12	ns
$t_{PDLHB}$	Propagation Delay to a Logical "1" from A Port to B Port	$CD = 0.4V$ , $T/\bar{R} = 2.4V$ (Figure 1) $R_1 = 100\Omega$ , $R_2 = 1k$ , $C_1 = 300pF$	15	20	ns
		$R_1 = 667\Omega$ , $R_2 = 5k$ , $C_1 = 45pF$	9	14	ns
$t_{PLZB}$	Propagation Delay from a Logical "0" to 3-State from CD to B Port	$A_0$ to $A_7 = 2.4V$ , $T/\bar{R} = 2.4V$ (Figure 3) $S_3 = 1$ , $R_5 = 1k$ , $C_4 = 15pF$	13	18	ns
$t_{PHZB}$	Propagation Delay from a Logical "1" to 3-State from CD to B Port	$A_0$ to $A_7 = 0.4V$ , $T/\bar{R} = 2.4V$ (Figure 3) $S_3 = 0$ , $R_5 = 1k$ , $C_4 = 15pF$	8	15	ns
$t_{PZLB}$	Propagation Delay from 3-State to a Logical "0" from CD to B Port	$A_0$ to $A_7 = 2.4V$ , $T/\bar{R} = 2.4V$ (Figure 3) $S_3 = 1$ , $R_5 = 100\Omega$ , $C_4 = 300pF$	25	35	ns
		$S_3 = 1$ , $R_5 = 667\Omega$ , $C_4 = 45pF$	16	25	ns
		$A_0$ to $A_7 = 0.4V$ , $T/\bar{R} = 2.4V$ (Figure 3) $S_3 = 0$ , $R_5 = 1k$ , $C_4 = 300pF$	22	35	ns
$t_{PZHB}$	Propagation Delay from 3-State to a Logical "1" from CD to B Port	$S_3 = 0$ , $R_5 = 5k$ , $C_4 = 45pF$	14	25	ns
<b>TRANSMIT RECEIVE MODE SPECIFICATIONS</b>					
$t_{TRL}$	Propagation Delay from Transmit Mode to Receive a Logical "0", $T/\bar{R}$ to A Port	$CD = 0.4V$ (Figure 2) $S_1 = 1$ , $R_4 = 100\Omega$ , $C_3 = 5pF$ $S_2 = 1$ , $R_3 = 1k$ , $C_2 = 30pF$	23	35	ns
$t_{TRH}$	Propagation Delay from Transmit Mode to Receive a Logical "1", $T/\bar{R}$ to A Port	$CD = 0.4V$ (Figure 2) $S_1 = 0$ , $R_4 = 100\Omega$ , $C_3 = 5pF$ $S_2 = 0$ , $R_3 = 5k$ , $C_2 = 30pF$	22	35	ns
$t_{RTL}$	Propagation Delay from Receive Mode to Transmit a Logical "0", $T/\bar{R}$ to B Port	$CD = 0.4V$ (Figure 2) $S_1 = 1$ , $R_4 = 100\Omega$ , $C_3 = 300pF$ $S_2 = 1$ , $R_3 = 300\Omega$ , $C_2 = 5pF$	26	35	ns
$t_{RTH}$	Propagation Delay from Receive Mode to Transmit a Logical "1", $T/\bar{R}$ to B Port	$CD = 0.4V$ (Figure 2) $S_1 = 0$ , $R_4 = 1k$ , $C_3 = 300pF$ $S_2 = 0$ , $R_3 = 300\Omega$ , $C_2 = 5pF$	27	35	ns

- Notes: 1. All typical values given are for  $V_{CC} = 5.0V$  and  $T_A = 25^\circ C$ .  
2. Only one output at a time should be shorted.

FUNCTION TABLE

Inputs	Conditions		
Chip Disable	0	0	1
Transmit/Receive	0	1	X
A Port	Out	In	HI-Z
B Port	In	Out	HI-Z

AC ELECTRICAL CHARACTERISTICS ( $V_{CC} = 5.0V$ ,  $T_A = 25^\circ C$ )

Parameters	Description	Test Conditions	Typ (Note 1)	Max	Units
<b>A PORT DATA/MODE SPECIFICATIONS</b>					
$t_{PDHLA}$	Propagation Delay to a Logical "0" from B Port to A Port	$CD = 0.4V$ , $T/\bar{R} = 0.4V$ (Figure 1) $R_1 = 1k$ , $R_2 = 5k$ , $C_1 = 30pF$	14	18	ns
$t_{PDLHA}$	Propagation Delay to a Logical "1" from B Port to A Port	$CD = 0.4V$ , $T/\bar{R} = 0.4V$ (Figure 1) $R_1 = 1k$ , $R_2 = 5k$ , $C_1 = 30pF$	13	18	ns
$t_{PLZA}$	Propagation Delay from a Logical "0" to 3-State from CD to A Port	$B_0$ to $B_7 = 0.4V$ , $T/\bar{R} = 0.4V$ (Figure 3) $S_3 = 1$ , $R_5 = 1k$ , $C_4 = 15pF$	11	15	ns
$t_{PHZA}$	Propagation Delay from a Logical "1" to 3-State from CD to A Port	$B_0$ to $B_7 = 2.4V$ , $T/\bar{R} = 0.4V$ (Figure 3) $S_3 = 0$ , $R_5 = 1k$ , $C_4 = 15pF$	8	15	ns
$t_{PZLA}$	Propagation Delay from 3-State to a Logical "0" from CD to A Port	$B_0$ to $B_7 = 0.4V$ , $T/\bar{R} = 0.4V$ (Figure 3) $S_3 = 1$ , $R_5 = 1k$ , $C_4 = 30pF$	27	35	ns
$t_{PZHA}$	Propagation Delay from 3-State to a Logical "1" from CD to A Port	$B_0$ to $B_7 = 2.4V$ , $T/\bar{R} = 0.4V$ (Figure 3) $S_3 = 0$ , $R_5 = 5k$ , $C_4 = 30pF$	19	25	ns
<b>B PORT DATA/MODE SPECIFICATIONS</b>					
$t_{PDHLB}$	Propagation Delay to a Logical "0" from A Port to B Port	$CD = 0.4V$ , $T/\bar{R} = 2.4V$ (Figure 1) $R_1 = 100\Omega$ , $R_2 = 1k$ , $C_1 = 300pF$	18	23	ns
		$R_1 = 667\Omega$ , $R_2 = 5k$ , $C_1 = 45pF$	11	18	ns
$t_{PDLHB}$	Propagation Delay to a Logical "1" from A Port to B Port	$CD = 0.4V$ , $T/\bar{R} = 2.4V$ (Figure 1) $R_1 = 100\Omega$ , $R_2 = 1k$ , $C_1 = 300pF$	16	23	ns
		$R_1 = 667\Omega$ , $R_2 = 5k$ , $C_1 = 45pF$	11	18	ns
$t_{PLZB}$	Propagation Delay from a Logical "0" to 3-State from CD to B Port	$A_0$ to $A_7 = 0.4V$ , $T/\bar{R} = 2.4V$ (Figure 3) $S_3 = 1$ , $R_5 = 1k$ , $C_4 = 15pF$	13	18	ns
$t_{PHZB}$	Propagation Delay from a Logical "1" to 3-State from CD to B Port	$A_0$ to $A_7 = 2.4V$ , $T/\bar{R} = 2.4V$ (Figure 3) $S_3 = 0$ , $R_5 = 1k$ , $C_4 = 15pF$	8	15	ns
$t_{PZLB}$	Propagation Delay from 3-State to a Logical "0" from CD to B Port	$A_0$ to $A_7 = 0.4V$ , $T/\bar{R} = 2.4V$ (Figure 3) $S_3 = 1$ , $R_5 = 100\Omega$ , $C_4 = 300pF$	32	40	ns
		$S_3 = 1$ , $R_5 = 667\Omega$ , $C_4 = 45pF$	16	22	ns
$t_{PZHB}$	Propagation Delay from 3-State to a Logical "1" from CD to B Port	$A_0$ to $A_7 = 2.4V$ , $T/\bar{R} = 2.4V$ (Figure 3) $S_3 = 0$ , $R_5 = 1k$ , $C_4 = 300pF$	26	35	ns
		$S_3 = 0$ , $R_5 = 5k$ , $C_4 = 45pF$	14	22	ns
<b>TRANSMIT RECEIVE MODE SPECIFICATIONS</b>					
$t_{TRL}$	Propagation Delay from Transmit Mode to Receive a Logical "0", $T/\bar{R}$ to A Port	$CD = 0.4V$ (Figure 2) $S_1 = 0$ , $R_4 = 100\Omega$ , $C_3 = 5pF$ $S_2 = 1$ , $R_3 = 1k$ , $C_2 = 30pF$	30	40	ns
$t_{TRH}$	Propagation Delay from Transmit Mode to Receive a Logical "1", $T/\bar{R}$ to A Port	$CD = 0.4V$ (Figure 2) $S_1 = 1$ , $R_4 = 100\Omega$ , $C_3 = 5pF$ $S_2 = 0$ , $R_3 = 5k$ , $C_2 = 30pF$	28	40	ns
$t_{RTL}$	Propagation Delay from Receive Mode to Transmit a Logical "0", $T/\bar{R}$ to B Port	$CD = 0.4V$ (Figure 2) $S_1 = 1$ , $R_4 = 100\Omega$ , $C_3 = 300pF$ $S_2 = 0$ , $R_3 = 300\Omega$ , $C_2 = 5pF$	31	40	ns
$t_{RTH}$	Propagation Delay from Receive Mode to Transmit a Logical "1", $T/\bar{R}$ to B Port	$CD = 0.4V$ (Figure 2) $S_1 = 0$ , $R_4 = 1k$ , $C_3 = 300pF$ $S_2 = 1$ , $R_3 = 300\Omega$ , $C_2 = 5pF$	28	40	ns

- Notes: 1. All typical values given are for  $V_{CC} = 5.0V$  and  $T_A = 25^\circ C$ .  
2. Only one output at a time should be shorted.

**DEFINITION OF FUNCTIONAL TERMS**

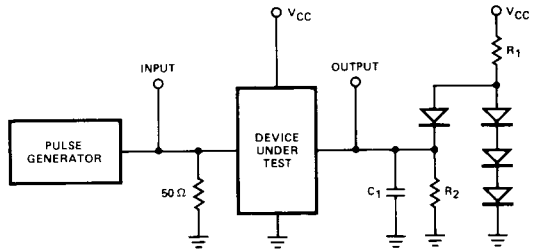
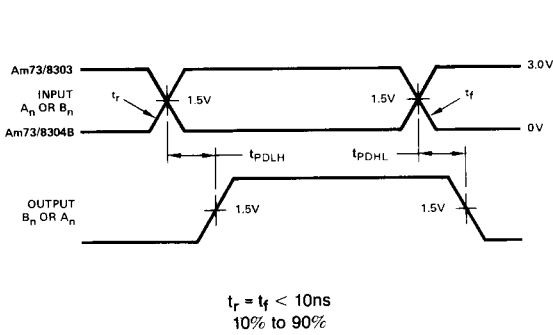
**A<sub>0</sub>-A<sub>7</sub>** A port inputs/outputs are receiver output drivers when  $T/\bar{R}$  is LOW and are transmit inputs when  $T/\bar{R}$  is HIGH.

**B<sub>0</sub>-B<sub>7</sub>** B port inputs/outputs are transmit output drivers when  $T/\bar{R}$  is HIGH and receiver inputs when  $T/\bar{R}$  is LOW.

**CD** Chip Disable forces all output drivers into 3-state when HIGH (same function as active LOW chip select,  $\bar{CS}$ ).

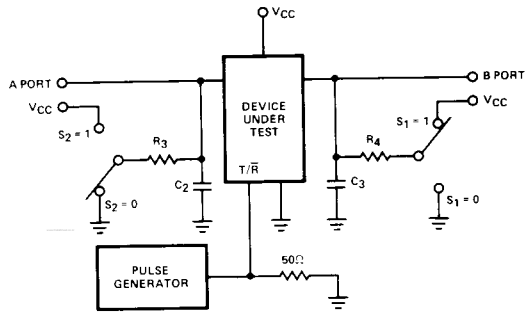
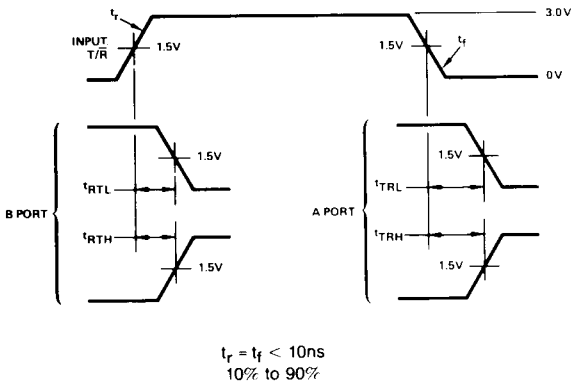
**T/ $\bar{R}$**  Transmit/Receive direction control determines whether A port or B port drivers are in 3-state. With  $T/\bar{R}$  HIGH A port is the input and B port is the output. With  $T/\bar{R}$  LOW A port is the output and B port is the input.

### SWITCHING TIME WAVEFORMS AND AC TEST CIRCUITS



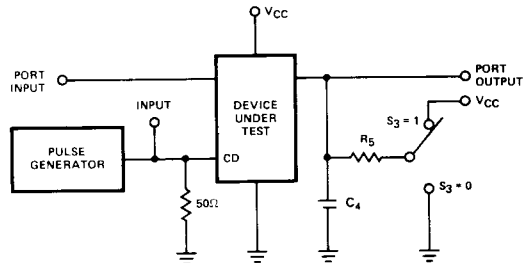
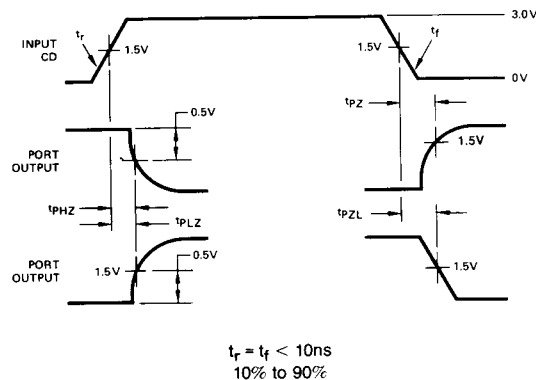
Note:  $C_1$  includes test fixture capacitance.

Figure 1. Propagation Delay from A Port to B Port or from B Port to A Port.



Note:  $C_2$  and  $C_3$  include test fixture capacitance.

Figure 2. Propagation Delay from  $T/\bar{R}$  to A Port or B Port.

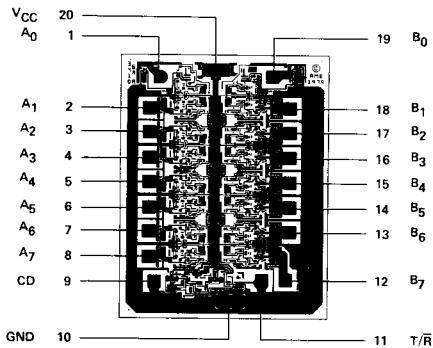


Note:  $C_4$  includes test fixture capacitance.  
Port input is in a fixed logical condition.

Figure 3. Propagation Delay from CD to A Port or B Port.

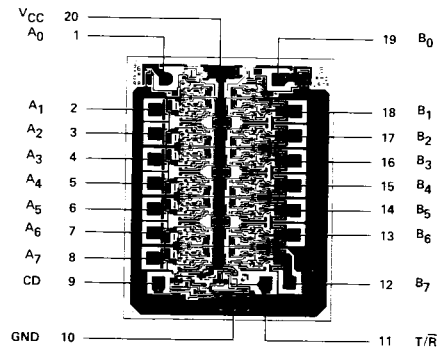
## Metallization and Pad Layouts

Am73/8303



DIE SIZE .069" X .089"

Am73/8304B



DIE SIZE .069" X .089"

## ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Am73/8303 Order Number	Am73/8304B Order Number	Package Type (Note 1)	Operating (Note 2)	Screening Level (Note 3)
DP7303J	DP7304BJ	D-20	M	C-3
DP7303JB	DP7304BJB	D-20	M	B-3
DP8303J	DP8304BJ	D-20	C	C-1
DP8303JB	DP8304BJB	D-20	C	B-1
DP8303N	DP8304BN	P-20	C	C-1
DP8303NB	DP8304BNB	P-20	C	B-1
AM7303X	AM7304BX	Dice	M	Visual inspection to MIL-STD-883 Method 2010B.
AM8303X	AM8304BX	Dice	C	

## Notes:

1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads.
2. C = 0 to 70°C,  $V_{CC}$  = 4.75 to 5.25V, M = -55 to +125°C,  $V_{CC}$  = 4.50 to 5.50V.
3. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.